CLAIM AMENDMENTS

Amend Claim 1 as follows:

Claim 1. (Twice Amended) A current sense integrated circuit, comprising:

an amplifier circuit for receiving and amplifying a differential analog input signal at a first voltage level containing current sense information, wherein the amplifier circuit includes a circuit to minimize inherent offset voltage temperature [offset] drift, comprising a first pair of mirrored MOSFET's, such that the circuit has an offset voltage which is equal to the difference between the respective gate-to-source voltages of the MOSFET's and remains constant over temperature variations;

a pulse width modulator circuit for converting the differential analog input signal to a pulse width modulated signal at the first voltage level; and

a level shift circuit for converting the pulse width modulated signal from the first voltage level to a second voltage level. [; and

a recovery circuit for reconstruction the analog input signal at the second voltage level.]

Cancel Claim 2.

Add new Claims 5-8 as follows:

Claim 5. The current sense integrated circuit of claim 1, wherein said first pair of mirrored MOSFET's receive said differential analog input signal.

Claim 6. The current sense integrated circuit of claim 1, further comprising a second pair of mirrored MOSFET's connected respectively in series with said first pair of mirrored MOSFET's for equalizing current and biasing of said first pair.

Claim 7. A current sense integrated circuit as claimed in claim 1, wherein said amplifier circuit has a differential input stage for receiving said differential analog input signal, said differential

input stage having two branches including inverting and non-inverting inputs, respectively, and said first pair of mirrored MOSFET's being connected in said two branches, respectively.

Claim 8. A current sense integrated circuit as claimed in claim 7, further comprising an output stage of said amplifier circuit, and a further matched pair of MOSFET's respectively connected for controlling current in said input stage and said output stage.